IN THE SPECIFICATION

Please make the following amendment to the paragraph on page 1, lines 10-12:

The present invention relates to processors. In one example, the present invention relates to methods and apparatus for processors handling an ~~and~~ event such as a fault or reset event.

Please make the following amendments to the paragraph on page 11, lines 4-15:

In some examples, it may be possible to specially configure ~~configured~~ circuitry to invalidate all the lines of a cache 531 including all instruction cache lines and all data cache lines. However, providing such specialized circuitry can be resource intensive, particularly for programmable chips. Consequently, the techniques of the present invention envision providing specialized circuitry to invalidate a limited number of lines and instruction cache 531. In one example, a single line including several instructions is invalidated. The several instructions are then used to initiate a software routine to invalidate the remaining lines in the cache 531. In one example, the software routine invalidates only the instruction cache lines. In another example, lines including both instruction cache lines in data cache lines are invalidated. Any logic or mechanism used to invalidate a reset address line is referred to herein as reset address line invalidate ~~circuitry~~ circuitry.